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Claims

[c1] A method of forming a strained silicon-on-insulator structure (10), the method comprising the steps of:
forming a silicon layer (12) on a strain-inducing layer (22) so as to form a multilayer structure (18), the strain-inducing layer (22) having a different lattice constant than silicon so that the silicon layer (12) is strained as a result of a lattice mismatch with the strain-inducing layer (22);
bonding the multilayer structure (18) to a substrate (24) so that an insulating layer (14) is between the strained silicon layer (12) and the substrate (24), the strained silicon layer (12) directly contacting the insulating layer (14); and then
removing the strain-inducing layer (22) to expose a surface of the strained silicon layer (12) and to yield a strained silicon-on-insulator structure (10) comprising the substrate (24), the insulating layer (14) on the substrate (24), and the strained silicon layer (12) on the insulating layer (14).

[c2] A method according to claim 1, wherein the substrate (24) is formed of a semiconductor material.

[c3] A method according to claim 1, wherein the strain-inducing layer (22) is formed of a SiGe alloy, and the strained silicon layer (12) is under tensile strain.

[c4] A method according to claim 1, wherein the strained silicon layer (12) is formed by epitaxial growth on the strain-inducing layer (22).

[c5] A method according to claim 1, wherein the insulating layer (14) is on the substrate (24), and the bonding step comprises bonding the insulating layer (14) of the substrate (24) to the strained silicon layer (12) of the multilayer structure (18).

[c6] A method according to claim 1, wherein the insulating layer (14b) is on the substrate (24), the multilayer structure (16) comprises the strain-inducing layer (22), the strained silicon layer (12) on and contacting the strain-inducing layer (22), and a second insulating layer (14a) on the strained silicon layer (12), and the bonding step comprises bonding the insulating layer (14b) of the substrate (24) to the second insulating layer (14a) of the multilayer structure (18).

[c7] A method according to claim 1, wherein the multilayer structure (18) comprises the strain-inducing layer (22), the strained silicon layer (12) on and contacting the

strain-inducing layer (22), and the insulating layer (14) on the strained silicon layer (12), and the bonding step comprises bonding the insulating layer (14) of the multi-layer structure (18) to the substrate (24).

[c8] A method according to claim 1, wherein the multilayer structure (18) comprises the strain-inducing layer (22), the strained silicon layer (12) on and contacting the strain-inducing layer (22), the insulating layer (14) on the strained silicon layer (12), and a semiconductor layer (24a) on the insulating layer (14), and the bonding step comprises bonding the semiconductor layer (24a) of the multilayer structure (18) to the substrate (24b).

[c9] A method according to claim 8, wherein the substrate (24,24a,24b) is formed of a semiconductor material.

[c10] A method according to claim 1, wherein the removing step comprises one or more techniques chosen from the group consisting of chemical-mechanical polishing, wafer cleaving, and chemical etching selective to silicon.

[c11] A method according to claim 1, further comprising the step of forming an IC device (40,50) in the surface of the strained silicon layer (12).

[c12] A method according to claim 11, wherein the step of forming the IC device (40,50) comprises the steps of

forming source and drain regions (26,28) in the surface of the strained silicon layer (12) so that the strained silicon layer (12) defines a channel (30) between the source region (26,28) and the drain region (26,28), the channel (30) being in direct contact with the insulating layer (14).

[c13] A method of forming a MOSFET device (40,50), the method comprising the steps of:
epitaxially growing a silicon layer (12) on a SiGe layer (22) so as to form a multilayer structure (18), the SiGe layer (22) having a different lattice constant than silicon so that the silicon layer (12) is under tensile strain as a result of a lattice mismatch with the SiGe layer (22);
bonding the multilayer structure (18) to a substrate (20) comprising a semiconductor layer (24), the bonding step resulting in the presence of an insulating layer (14) between the strained silicon layer (12) and the substrate (20), the strained silicon layer (12) directly contacting the insulating layer (14);
removing the SiGe layer (22) to expose a surface of the strained silicon layer (12) and to yield a strained silicon-on-insulator structure (10) comprising the substrate (20), the insulating layer (14) on the substrate (20), and the strained silicon layer (12) on the insulating layer (14); and then
forming an IC device (40,50) in the surface of the

strained silicon layer (12).

[c14] A method according to claim 13, wherein the substrate (20) comprises the insulating layer (14) and the semiconductor layer (24), and the bonding step comprises bonding the insulating layer (14) of the substrate (20) to the strained silicon layer (12) of the multilayer structure (18).

[c15] A method according to claim 13, wherein the substrate (20) comprises the insulating layer (14b) and the semiconductor layer (24), the multilayer structure (18) comprises the SiGe layer (22), the strained silicon layer (12) on and contacting the SiGe layer (22), and a second insulating layer (14a) on the strained silicon layer (12), and the bonding step comprises bonding the insulating layer (14b) of the substrate (20) to the second insulating layer (14a) of the multilayer structure (18).

[c16] A method according to claim 13, wherein the multilayer structure (18) comprises the SiGe layer (22), the strained silicon layer (12) on and contacting the SiGe layer (22), and the insulating layer (14) on the strained silicon layer (12), and the bonding step comprises bonding the insulating layer (14) of the multilayer structure (18) to the semiconductor layer (24) of the substrate (20).

[c17] A method according to claim 13, wherein the multilayer structure (18) comprises the SiGe layer (22), the strained silicon layer (12) on and contacting the SiGe layer (22), the insulating layer (14) on the strained silicon layer (12), and a second semiconductor layer (24a) on the insulating layer (14), and the bonding step comprises bonding the semiconductor layer (24b) of the substrate (20) to the second semiconductor layer (24a) of the multilayer structure (18).

[c18] A method according to claim 13, wherein the removing step comprises one or more techniques chosen from the group consisting of chemical-mechanical polishing, wafer cleaving, and chemical etching selective to silicon.

[c19] A method according to claim 13, wherein the step of forming the IC device (40,50) comprises forming source and drain regions (26,28) in the surface of the strained silicon layer (12) so that the strained silicon layer (12) defines a channel (30) between the source region (26,28) and the drain region (26,28), the channel (30) being in direct contact with the insulating layer (14).

[c20] A method according to claim 19, further comprising the step of using the semiconductor layer (24) to form a gate electrode (36) separated from the channel (30) by the insulating layer (14).

[c21] A method according to claim 19, further comprising the steps of forming a gate oxide (32) on the surface of the strained silicon layer (12), and forming a gate electrode (34) on the gate oxide (32).

[c22] A method according to claim 19, further comprising the steps of:
using the semiconductor layer (24) to form a first gate electrode (36) separated from the channel (30) by the insulating layer (14);
forming a gate oxide (32) on the surface of the strained silicon layer (12); and
forming a second gate electrode (34) on the gate oxide (32);
wherein the method yields a double-gate MOSFET (50).

[c23] A method according to claim 13, wherein the SiGe layer (22) is formed of a SiGe alloy having the lattice constant of about 0.2 to about 2 percent larger than the lattice constant of silicon.